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Building Flexible SoCs

Menta Adaptive DSP Core

Menta® Origami Designer and Programmer provide an integrated environment for implementing users design using Menta embedded FPGAs IPs. Menta provide to its customer the possibility to infer automatically DSP Core hard blocks to improve their PPA.

Key features and benefits

- Automatic inference of Adaptive DSP block
- Possibility to define the physical size of the DSP
- Possibility to define the Multiplier and the ALU size
- Possibility to add a FIR SRL engine state machine and coefficients
- DSP can be cascaded to optimize routing
- Programmable
- Dynamically reconfigurable allowing change of behavior at each clock cycle
- Signed multiplier and accumulator
- Fully pipelined
- Implemented has a hard block within Menta eFPGA IP

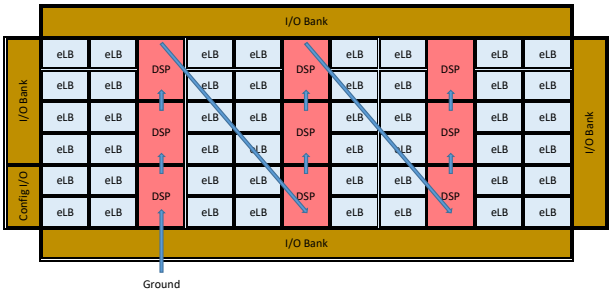
Adaptive Digital Signal Processor (DSP)

Create the most adaptive physical DSP

Menta synthesis tool is capable of automatically inferring DSP from any behavioral RTL code written in VHDL, Verilog or SystemVerilog code. The Adaptive Menta DSP solution allow users to implement the DSP operand size that better suits the hardware requirement.

The DSP operating modes are programmable through the Bitstream

Large multipliers can be implemented by cascading The DSP without requiring any routing through the switch box.

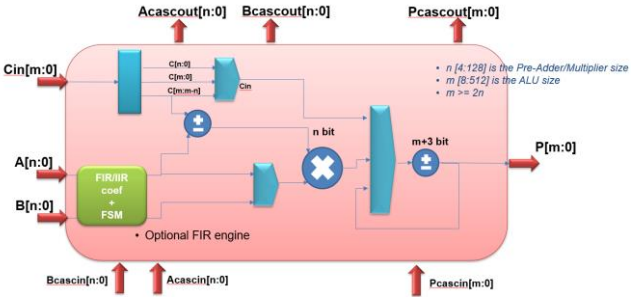


The DSP is also dynamically reconfigurable The operating mode may also be controlled at clock cycle level using application control signals.

The DSP is fully registered with up to two registers levels on A and B input, one register level on C and D (Independent). All internal operation (pre-adder, multiplier and accumulator) are optionally registered.

DSP Core

The DSP core is a signed multiplier with signed accumulator. The multiplier has a by passable signed pre-adder. For unsigned operation, the multiplier precision is lowered by 1.



The adaptive DSP block enables efficient implementation within Menta eFPGA of arithmetic algorithm, including, but not limited to: Multiplication, Multiplication–accumulation, Pre-add – Multiplication – Accumulation, Complex multipliers, FIR filters, Fast Fourier Transform, Large multiplier, Shift Register Lookup table (SRL) , convolution functions.

Fir Engine

FIR algorithms are composed of multipliers, adders and registers. As there are a number of different FIR architectures, It is important to understand the real application and performances requirements to choose the best hardware architecture when implementing a FIR.

Menta adaptive DSP optionally embeds all the required logic to implement FIR filter **without requiring the use of external LUT resources**. This includes the required SRL, state machine and coefficient involved in the implementation.

Menta FIR generator generates RTL code of an optimized FIR using **Menta Adaptive DSP**. The range of the FIR supported can be set between 4 and 512 taps. Users can define the number of DSP they want within their architecture depending on their target : area or Frequency. The Bus size and ALU size can also be defined.

Example 1: Fir 5 TAPs

Using **Menta FIR generator** , we have generated the RTL code of a FIR with 5 TAPs using only one **Menta Adaptive DSP and its FIR engine.** At each clock cycle only one sum of product is calculated. The final result is available after 5 clock results.

Implementation results using Technology node TSMC 28 HPC ; worst case 0.81v , 125 C, are:

Area (mm²)	Internal DSP Frequency (GHz)
0.08	2.2

Example2 : FIR with 21 Taps with symmetrical coefficients

Using **Menta FIR generator**, we have generated the RTL code of a FIR with 21 Taps, symmetrical coefficients using an optimized structure of 11 TAPs. The FIR has been implemented using only one **Menta Adaptive DSP and its FIR engine** .

Rather than doing : A1*C1 +A2*C2+…+A20*C2+A21*C1, we have been using the **Menta Adaptive DSP pre-adder** to optimize the structure (A1+A21)*C1 + (A2+A20)*C2 +….. (This approach could also be used with asymmetrical coefficients: (A1-A21)*C1 +… Coefficients are opposed rather than equal)

Implementation results using Technology node TSMC 28 HPC ; worst case 0.81v , 125 C, are :

Area (mm²)	Internal DSP Frequency (GHz)
0.08	1.7

Whitepaper on Menta adaptive DSP, Datasheets, Menta Starter Pack training & evaluation software as well as TSMC 28HPC+ evaluation board are available.

For more information visit our website at: www.menta-efpga.com